IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

REDACTED
PUBLIC VERSION

POWER INTEGRATIONS, INC.,

Plaintiff,

v.

FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION,

Defendants.

C.A. No. 04-1371-JJF

COMBINED APPENDIX TO DEFENDANTS': (i) OPENING POST-TRIAL BRIEF IN SUPPORT OF THEIR ASSERTION THAT THE PATENTS-IN-SUIT ARE UNENFORCEABLE DUE TO INEQUITABLE CONDUCT; AND (ii) PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW REGARDING THE UNENFORCEABILITY OF THE PATENTS-IN-SUIT DUE TO INEQUITABLE CONDUCT

(VOLUME I of V)

ASHBY & GEDDES
Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Lauren E. Maguire (I.D. #4261)
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
302-654-1888

Attorneys for Defendants

Of Counsel:

G. Hopkins Guy, III
Vickie L. Feeman
Bas de Blank
Brian H. VanderZanden
Orrick, Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
(650) 614-7400

Dated: November 5, 2007

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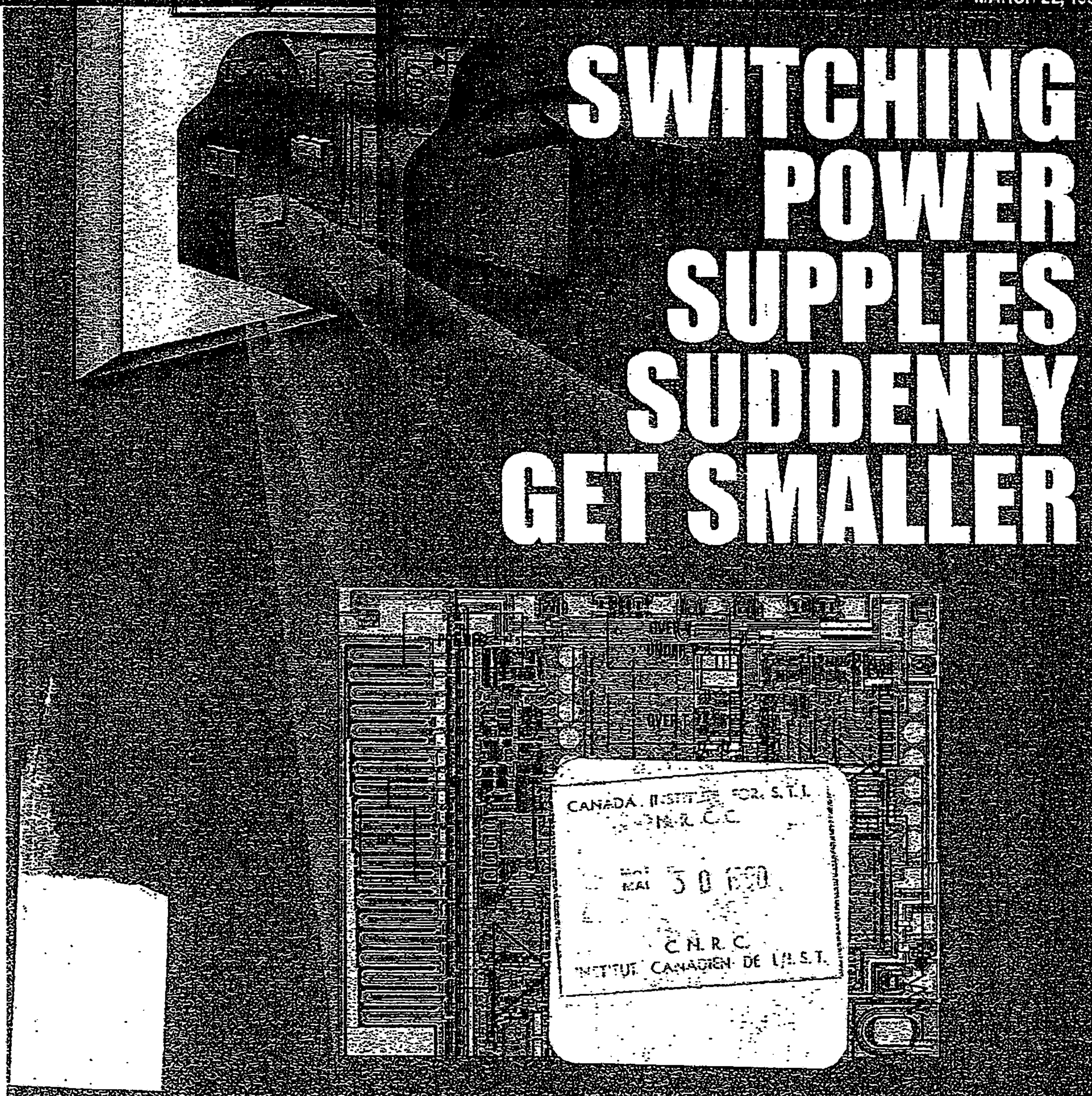

• SPECIAL REPORT: VHDL EMERGES AS A STANDARD

Case No. 04-1371-JJF
DEFT Exhibit No. DX 17
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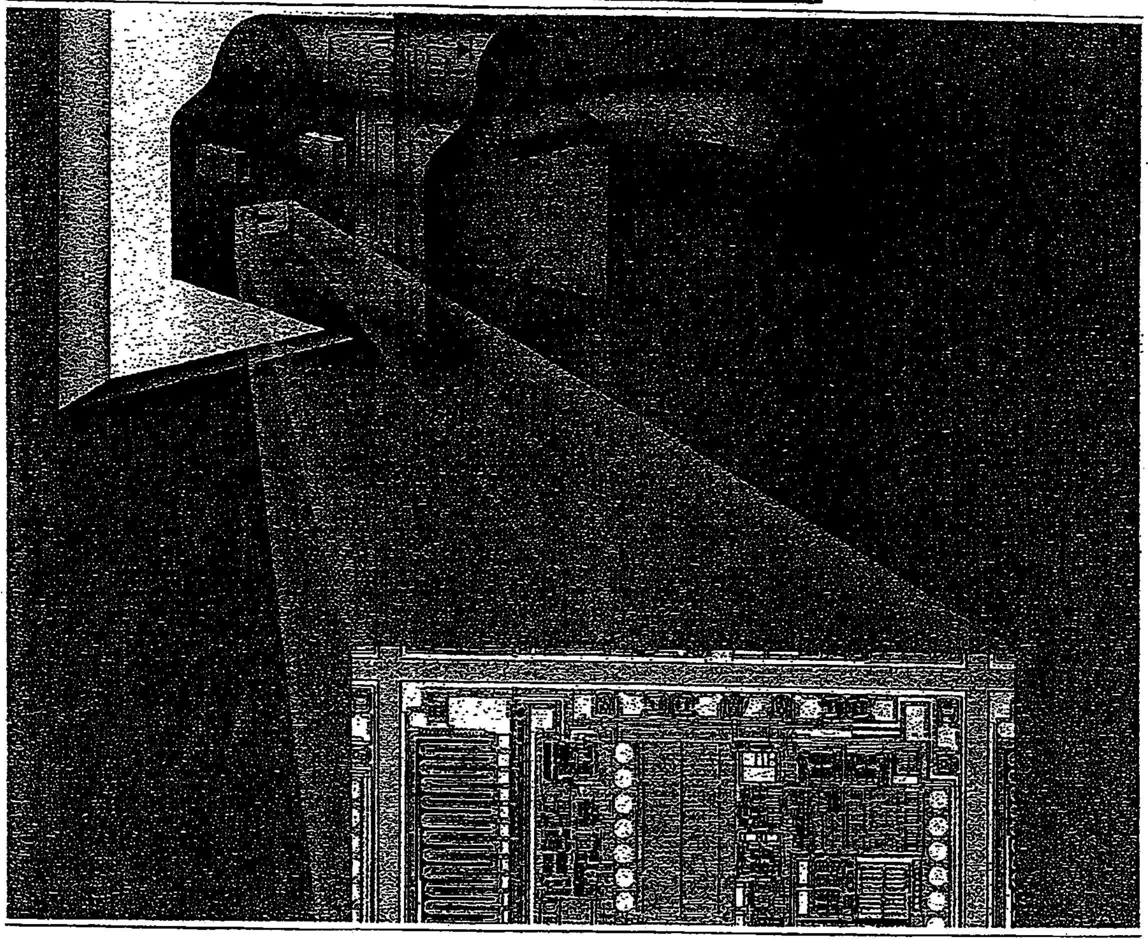

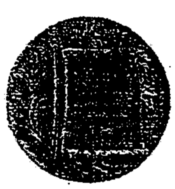

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ADDING A TRANSFORMER AND OTHER PASSIVE PARTS TO A POWER IC CREATES AN OFF-LINE 3-W SWITCHER THAT FITS IN A WALL PLUG.

OFF-LINE PWM SWITCHING REGULATOR IC HANDLES 3 W

FRANK GOODENOUGH

Now you can operate a battery-powered instrument, computer, modem or other small, low-power electronic device directly from the 115-V ac line without a bulky box to plug in. All that's required is Power Integration's PWR-SMP3 regulator IC to build a 3-W isolated switching power supply. Even if a rectifier bridge and filter are included, the supply's volume can be less than 0.5 $in.^3$ *(Fig. 1)*. Typical cost for such a supply in high-volume quantities is between $10 and $20 each, depending on its size and the number built.

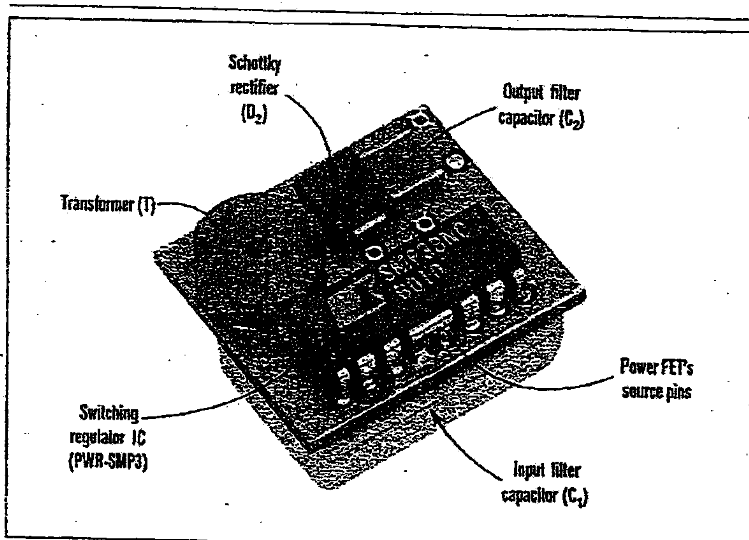
The PWR-SMP3 is built on the company's proprietary high-voltage CMOS process. This process puts 5-V logic and small-signal bipolar analog circuits on the same chip.

Housekeeping and/or startup circuits for large off-line supplies represent a typical application for regulators built with the PWR-SMP3. The supply can replace circuits that use bulky 115-V, 60-Hz transformers. It also lends itself to auxiliary outputs in multi-output supplies. In addition, it will simplify the design of multi-output custom circuits.

Other applications for the PWR-SMP3 include remotely located digital panel meters, credit-card readers, and remote, signal-conditioning circuits and modules. Essentially any low-power circuitry where 115 V ac is available can be powered. Because circuit voltage-isolation is a function of the transformer, not the chip, the PWR-SMP3 can even be used in medical instrumentation or factory-floor automation systems, such as programmable controllers.

Regulators akin to the PWR-SMP3 further the trend to distributed power applications. In such applications, a relatively high voltage (50 to 200 V) is piped around a large multicabinet system to reduce IR line losses. Dc-to-dc

COVER: OFF-LINE PWM SWITCHING REGULATOR IC



1. OCCUPYING a volume of just one-half cubic inch, this complete off-line switching regulator—built with Power Integrations PWR-SMP3 power IC in a DIP—controls up to 3 W.

converters on each system board reduce the high voltages to typical semiconductor voltage levels *(see* ELECTRONIC DESIGN, *Jan. 11, p. 88)*. These regulators can even be smaller because the bridge rectifier and input capacitor aren't needed. With the chip's 3-W rating, supplies could be built to typically deliver 200 mA at 15 V, 250 mA at 12 V, or 600 mA at 5 V. A pair of regulators could thus supply ±15-V power for a slew of op amps. Or one regulator could supply 600 mA of −5.2-V ECL power in a primarily CMOS system.

To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage-inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 *(Fig. 2)*. Packaged in a 16-pin DIP, the regulator is the supply's heart. Running at 1 MHz to minimize inductor size, the PWR-SMP3's controller section is optimized to implement a voltage-mode flyback circuit. Alternatively, other common pulse-width-modulated (PWM) regulator topologies may also be employed.

The chip's circuit includes all of the blocks needed for a basic PWM regulator and all of the self-protection blocks expected in today's controllers *(Fig. 2, again)*. The input dc voltage (200 V maximum) is applied to the CMOS power FET through the transformer and to a linear preregulator which drops it to the 6-V V_S required to run the control circuits during startup. Once the supply is up and running, the preregulator is turned off. The small-signal circuits on the chip are then powered from the "bootstrap"/feedback output from the transformer through the rectifier-filter formed by diode D_5 and capacitor C_5.

Bypass capacitor C_3 keeps switching noise out of the control circuitry. Diodes D_3 and D_4 snub Ldi/dt transients as the switch turns off. A fast, low-loss Schottky diode—D_2—rectifies the voltage across the isolated output winding of the transformer, which is filtered by C_2 to give 600 mA of regulated 5-V power. Virtually any other voltage can be generated by changing the secondary winding of the transformer.

The basic PWM circuit is conventional. The 0-to-50% duty-cycle pulses from the oscillator turn on the FET switch through the NAND-gate and the FET-gate driver. The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference between the supply's output voltage through the feedback path and the output of the 1.25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips and turns off the FET switch through the OR gate, PWM latch, NAND gate, and driver.

NO SELF-DESTRUCT

As noted earlier, the chip is loaded with self-protection features. To start, the FET switch is a sense, or mirror, FET with an output that feeds a small fraction of the total drain current through an on-chip current-sensing resistor, R_{sense}. The voltage developed across the resistor is applied to the current-limit comparator. When the drain current exceeds approximately 300 mA, the FET is quickly turned off.

When using this technique, voltage noise can be a problem because typical sense voltages run as low as 200 and 500 mV. Increasing the sense voltage tends to degrade the linear relationship between it and drain current. In this FET, however, proprietary compensation techniques raise the sense voltage while maintaining linearity.

On the input side of the chip, overvoltage and undervoltage (OV/UV) lockout circuits ensure that the input voltage and the 6-V internal (bias) supply are within the required limits before the supply will operate. Input OV lockout is particularly useful in off-line applications where surges or high-energy spikes are apt to be present. The supply shuts down during the transient and starts up when the input returns to the proper range. The OV/UV levels are programmed by the divider formed by resistors R_1 and R_2. Shutdown also occurs when the internal bias voltage is too low for proper circuit operation. Hysteresis in these circuits ensures reliable, noise-free operation. The chip can either be shut down or kept from turning on by holding the OV/UV pin low. Turn-on can be delayed—for example, if turn-on of multiple supplies must be sequenced—by hanging a capacitor on the pin.

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COVER: OFF-LINE PWM SWITCHING REGULATOR IC

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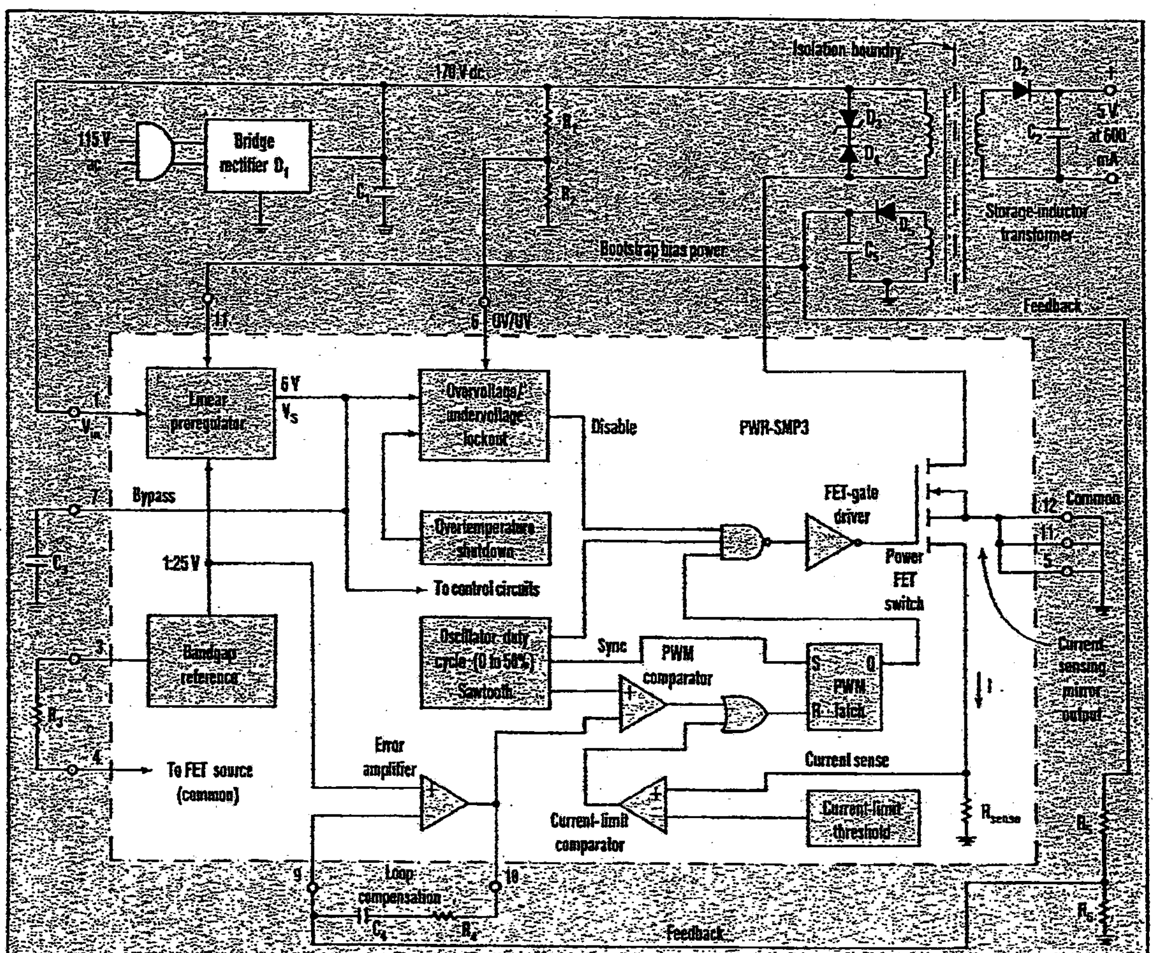
The soft-start circuit consists of a current source and an internal capacitor connected to an intermediate stage of the error amplifier. Until the capacitor is fully charged, the error amplifier output voltage is clamped low, limiting the duty cycle and peak current of the switch during startup. Once the capacitor is fully charged, the amplifier takes over and regulates the output voltage. All shutdown and lockout modes discharge this capacitor, ensuring that the supply always starts from a known state. The over-temperature shutdown circuit turns the switch off when the chip's temperature reaches between 125° and 175°C. Built-in hysteresis makes sure the temperature drops at least 45°C before the switch comes on again.

SUPERIOR CMOS

The chip will operate with input voltages between 36 and 200 V, adapting it to 48-V telecommunications applications. While oscillating at 1 MHz, the chip's quiescent current is just 4 mA. The FET switch's on-resistance is typically 14 Ω, and output capacitance is a low 8 pF. Rise and fall times of the output are typically 40 ns, with an input voltage of 160 V and a drain current of 200 mA.

In its 16-pin, plastic modified bat-wing package, the PWR-SMP3 can operate to 70°C. In the bat-wing package, which is designed to remove heat, the four center pins (4, 5, 12, and 13) are part of the copper lead frame on which the die is mounted. They're tied to the source of the FET and may be used as ground connections. Resistor R_3 is connected between pins 3 and 4 to set the internal operating currents. A separate bond wire connects pin 4 to the chip to minimize the effects of noise on the ground lines.

Power Integrations' process, in which lateral CMOS FETs are used for power switches instead of vertical DMOS FETs, brings more than



2. BY RECTIFYING AND FILTERING the 115-V ac line and applying it to the input of the PWR-SMP3 power IC through a storage-inductor/transformer, and by adding a few parts, a 5-V, 600-mA isolated and regulated PWM switching power supply can be created.

FCS1692109

COVER: OFF-LINE PWM SWITCHING REGULATOR IC

just low cost to high- and low-voltage silicon power ICs. To start, these devices can be built on virtually any, 3.5-μm mature CMOS line (similar to many companies, Power Integrations doesn't have a fabrication facility, so it uses multiple foundries). The 400-V FET switches from the process, comparable to so-called logic-level FETs, turn on hard with just 5 V of gate-to-source drive. This reduces gate-drive energy by a factor of four, significantly simplifying drive circuitry (at present, discrete logic-level FETs are limited in voltage-rating to about 100 V).

Moreover, Miller capacitance at the switch's gate is usually 1/3 that of similarly rated DMOSFETs, further reducing drive energy and raising switching speeds—which reduces inductor size. Running at 1 MHz, the switch in the PWR-SMP3 takes about 1 mW of drive power, while a typical similarly rated DMOSFET uses about 20 mW.

In addition to easier drive, the positive temperature coefficient of the on- resistance of these high-voltage CMOS power FETs is less than that of similarly rated discrete MOSFETs. At 150°C, the on-resistance of a DMOSFET is 2.5 times its 25°C value, while that of the CMOS IC switch is only twice as great.

The lateral CMOS construction also makes it possible for the package's metal tab to be connected to the source rather than to the switch's drain. This virtually eliminates displacement currents when compared with conventional technology where the drain (or collector) is connected to the case or tab.

These currents flowing through the system chassis and heat sinks contribute to system noise and common-mode electromagnetic-interference-conducted emissions. Lower noise levels may lead to less filtering to meet regulatory agency (FCC, VDE, CSA) requirements. To further increase switching speed, delays in the low-impedance driver were reduced by physically distributing the driver across the area occupied by the power FET itself.□

PRICE AND AVAILABILITY

In a 16-pin plastic DIP, the PWR-SMP3 goes for $6 in lots of 1000. High-volume prices are significantly lower. Small quantities are available from stock.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Art Fury or Doyle Slack, (415) 960-3572. CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

CIRCLE 97

ADDING A TRANSFORMER AND OTHER PASSIVE PARTS TO A POWER IC CREATES AN OFF-LINE 3-W SWITCHER THAT FITS IN A WALL PLUG.

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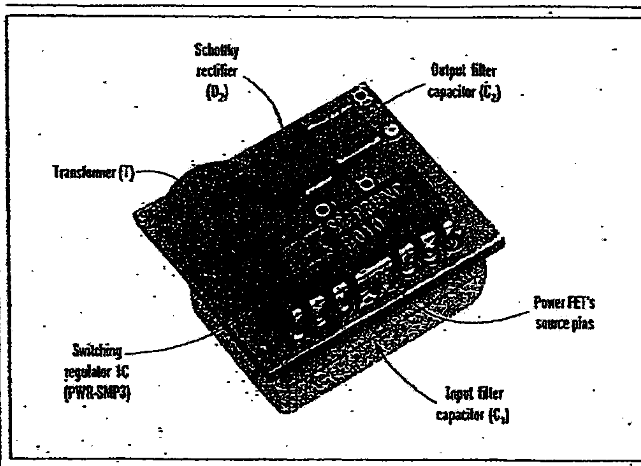

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SUPERIOR CMOS

The chip will operate with input voltages between 36 and 200 V, adapting it to 48-V telecommunications applications. While oscillating at 1 MHz, the chip's quiescent current is just 4 mA. The FET switch's on-resistance is typically 14 Ω, and output capacitance is a low 8 pF. Rise and fall times of the output are typically 40 ns, with an input voltage of 160 V and a drain current of 200 mA.

In its 16-pin, plastic modified bat-wing package, the PWR-SMP3 can operate to 70°C. In the bat-wing package, which is designed to remove heat, the four center pins (4, 5, 12, and 13) are part of the copper lead frame on which the die is mounted. They're tied to the source of the FET and may be used as ground connections. Resistor R_3 is connected between pins 3 and 4 to set the internal operating currents. A separate bond wire connects pin 4 to the chip to minimize the effects of noise on the ground lines.

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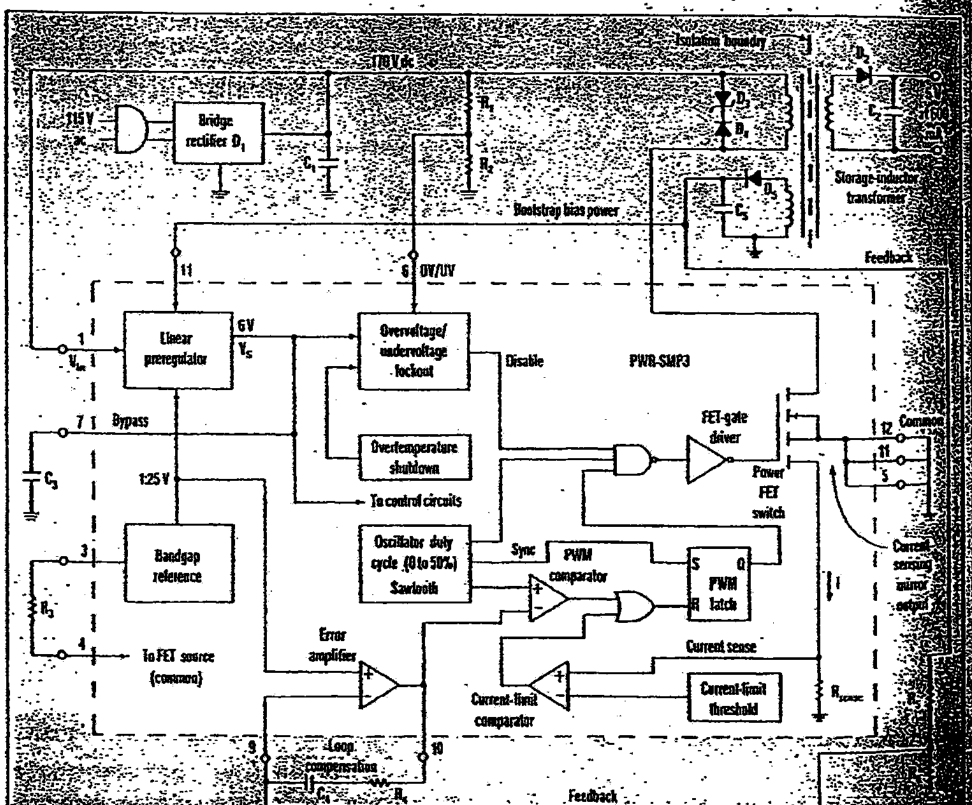

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Moreover, Miller capacitance at the switch's gate is usually 1/3 that of similarly rated DMOSFETs, further reducing drive energy and raising switching speeds—which reduces inductor size. Running at 1 MHz, the switch in the PWR-SMP3 takes about 1 mW of drive power, while a typical similarly rated DMOSFET uses about 20 mW.

In addition to easier drive, the positive temperature coefficient of the on- resistance of these high-voltage CMOS power FETs is less than that of similarly rated discrete MOSFETs. At 150°C, the on-resistance of a DMOSFET is 2.5 times its 25°C value, while that of the CMOS IC switch is only twice as great.

The lateral CMOS construction also makes it possible for the package's metal tab to be connected to the source rather than to the switch's drain. This virtually eliminates displacement currents when compared with conventional technology where the drain (or collector) is connected to the case or tab.

These currents flowing through the system chassis and heat sinks contribute to system noise and common-mode electromagnetic-interference-conducted emissions. Lower noise levels may lead to less filtering to meet regulatory agency (FCC, VDE, CSA) requirements. To further increase switching speed, delays in the low-impedance driver were reduced by physically distributing the driver across the area occupied by the power FET itself.□

PRICE AND AVAILABILITY

In a 16-pin plastic DIP, the PWR-SMP3 goes for $6 in lots of 1000. High-volume prices are significantly lower. Small quantities are available from stock.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Art Fury or Doyle Slack, (415) 960-3572. CIRCLE 511

HOW VALUABLE?	CIRCLE
HIGHLY	553
MODERATELY	554
SLIGHTLY	555

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TECHNICAL DIGEST

international ELECTRON DEVICES meeting

1983

WASHINGTON, DC

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1983 International Electron Devices Meeting
TECHNICAL DIGEST

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WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN

Michael Adler
General Chairman

Nino Masnari
Technical Program
Chairman

On behalf of the conference committee I would like to welcome you to the 1983 International Electron Devices Meeting in its return to Washington, D.C. Since its inception in 1955, the IEDM has been the largest and most prestigious international forum for the presentation of the latest research and development in the area of electron devices. Last year the IEDM moved to the West Coast in order to broaden the geographical base of the meeting. This experiment was met with rousing success attracting over 2,200 attendees with a not surprisingly large component from the Bay area (1,300). In the future the meeting will be alternating between the East and West coasts to best serve both the geographically diverse US and international community of electron device researchers.

In addition to broadening its geographical base, the IEDM has also broadened its experiential base by adding panel discussions and innovations such as the author contact sessions. For the 1983 IEDM, in its 29th year, this conscious attempt to better serve the meeting attendees continues with the addition of a Sunday short course on semiconductor processing. The short course will consist of four, one and a half hour sessions, on the subjects of optical lithography, dry etching, metallization, and CVD given by renowned experts in each area. The purpose of the course is to allow those in other areas of electron device research to become acquainted with the physical basis, expected results, and equipmental capabilities for key processing techniques. It is intended that the course will provide a technical bridge to the advanced processing developments presented in the IEDM itself.

This year the IEDM contains 27 sessions in the six categories of Electron Devices, Device Technology, Integrated Circuits, Detectors, Sensors and Displays, Quantum Electronics, and Electron Tubes. These sessions contain 185 papers selected from 456 submitted abstracts from 22 countries. These statistics reflect the technical and international breadth of the meeting as well as the usual intense competition for places on the contributed program. This competition also serves to guarantee that the technical quality of the meeting remains at the high standard set by previous IEDMs and expected by the meeting attendees. In addition to the contributed papers, three areas of broad interest and relevance are highlighted in plenary session invited papers on the topics of circuit and system limitations of ultra large-scale integration, optical communications devices and systems, and visible and infrared solid-state image sensors.

Four panel discussions will also be the forum for lively debate on the topics of the extendability of CMOS technology to the submicron era, the future of silicon on insulator substrates for VLSI, device and process modeling applied to VLSI design, and optoelectronic device needs for the future.

Rounding out the meeting will be a luncheon presentation on the topic of the Japanese 5th Generation Computer Project by Dr. Kazuhiro Fuchi, Director of the project. Dr. Fuchi will review the 5th Generation Project, a subject of intensive interest worldwide, indicating its present and future goals, present status, and placing in perspective the needs for advanced IC technology.

I would like to extend my thanks and congratulations to the Conference Committee for the outstanding job they have done in planning and organizing the 1983 IEDM and on behalf of the IEEE Electron Devices Society, which sponsors the IEDM, I want to extend my sincere appreciation for their dedicated and professional efforts.

In addition, the authors are to be commended for their efforts toward technical excellence in their papers. It is with pleasure that I welcome them and all attendees to the 1983 International Electron Devices Meeting.

Michael Adler
General Chairman

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Panel Moderator: Henry Kressel
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New York, NY

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